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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,647	10/08/2003	Jung Pill Kim	2003P5259US	6096

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,647	KIM ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-16* is/are rejected.

7)☒ Claim(s) *12 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "a method for reducing the sensitivity of a voltage generated internally to an integrated circuit device **to channel resistance** of switches utilized to adjust a level of the voltage" is confusing because it is not clear what this recitation is meant by. It is not clear how the resistance of switches can be channeled and how the "sensitivity of a voltage generated internally to an integrated circuit device " can be reduced. As understood by the examiner, figure 4 of the present application shows a voltage divider wherein the voltage at each node (NC, NP, NE, N1) can be selected by a system of switches. The "resistance of switches" cannot be "channeled" to anywhere.

Claims 2-6 are indefinite because of the technical deficiency of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-11 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Tedrow et al. (US Pat. 5,546,042).

Regarding claim 1, figure 2 and 5 of Tedrow show a method for "reducing the sensitivity of a voltage generated internally to an integrated circuit device to channel resistance of switches utilized to adjust a level of the voltage", the method comprising:

providing a voltage dividing circuit with a plurality of serially connected resistors (R3-Rk),

supplying the voltage dividing circuit with a reference voltage (Vref), resulting in a different voltage level at nodes of the voltage dividing circuit formed between the serially connected resistors; and

providing a plurality of switches (N2-Nk), to selectively couple an output node, on which the voltage is to be supplied, to a single node of the voltage dividing circuit.

Regarding claims 2 and 3, only one of the switches is turned on (closed) at a given time (col. 7, lines 38-39).

Regarding claim 4, the switches in figures 5 are controlled by signals stored in non-volatile elements (see figure 2, element 30, and col.3, lines 37-42).

Regarding claims 5, the control signals for switches (N2-Nk) are generated by a single element of the circuit: the "a control engine" (col. 7, lines 35-38).

Regarding claim 7, figure 2 and 5 of Tedrow show trimming circuit for use in adjusting a voltage generated internally to an integrated circuit device, comprising:

a plurality of switches (N2-Nk) to selectively couple an output node on which the voltage is supplied to a single one of a plurality of nodes of a voltage dividing circuit (divider (R3-Rk) wherein each node is at a different voltage level.

Regarding claim 8, figure 5 shows that a single switch is coupled between the output node (Vout) and each node of the voltage dividing circuit.

Regarding claim 9, the plurality of switches (N2-Nk) open and close in response to control signals generated as a function of states of one or more non-volatile storage elements (see figure 2, element 30, and col.3, lines 37-42).

Regarding claim 10, figure 3 of Tedrow shows the detail of the non-volatile memory device (30). The decoder (54) decodes data from memory array 50 (non-volatile) for generating control signals (col. 3, lines 37-45; col. 4, lines 27-46; col.7, lines 35-39).

Regarding claim 11, the number of switches (N2-Nk) is greater than the number of non-volatile storage elements (50).

Regarding claim 13, figures 2 and 5 of Tedrow shows a memory device comprising:

peripheral circuitry (39);

a plurality of memory cells in circuit (30);

a voltage generating circuit comprising a voltage divider circuit (R2-Rk) with a plurality of nodes, each at different voltage levels dependent on a reference voltage, and a plurality of switches (N2-Nk) to selectively couple an output node (Vout) of the voltage generating circuit with a single one of the voltage divider circuit nodes.

Regarding claims 14 and 15, the non-volatile memory element (30) generates signals for controlling the switches. The decoder is element (54) in figure 3.

Regarding claim 16, it is inherent that a negative voltage can be generated when (Vpp) is a negative voltage source.

Allowable Subject Matter

Claims 12, and 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 12, and 17-20 are objected to because the prior art of record fails to teach or fairly suggest a trimming circuit comprising at least one additional switch connected in parallel to one of the serially connected resistors as called for in claim 12; a dynamic random access memory and a negative voltage applied to the substrate of the transistors of the memory cells as called for in claims 16 and 17; the memory device is a dynamic random access memory device and the voltage generating circuit is configured to generate a voltage to be supplied to word lines of the memory cells via the peripheral circuitry as called for in claim 18; additional switches for selectively bypassing one or more serially connected resistive elements as called for in claim 19; and fuses for generating control signals for the plurality of switched and at least one additional switch as called for in claim 20.

Claim 6 would be allowable because the prior art of record fails to teach or fairly suggest a trimming circuit comprising providing one or more switches in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
07-23-04

TUAN T. LAM
PRIMARY EXAMINER